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Docket No.: HI-0004

PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Application of

Won Hyoung PARK

Serial No.: 09/578,511

Confirm. No.: 7993

Filed: May 26, 2000

For: A DEMODULATION APPARATUS OF A BASE STATION IN A CDMA
MOBILE COMMUNICATION SYSTEM

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: Group Art Unit: 2631
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: Examiner: Qutbuddin Ghulamali
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: Customer No.: 34610
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APPEAL BRIEF

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This Appeal Brief is submitted in support of the Notice of Appeal filed October 15, 2003.

REAL PARTY IN INTEREST

The party in interest is the assignee LG Information & Communications, Ltd.

RELATED APPEALS AND INTERFERENCES

The Appellant is unaware of any related appeals or interferences.

STATUS OF THE CLAIMS

This is an appeal from the final rejection dated July 15, 2003 of claims 1, 21-23, 25-29, 31-33, 35-39, 41 and 42. Claims 6-17 and 19-20 have been allowed. Claims 2-5, 24, 30, 34 and 40 have been objected to as being dependent on a rejected claim, but indicated as being otherwise allowable.

STATUS OF AMENDMENTS

All Amendments filed in this application have been entered. A correct copy of appealed claims 1, 21-23, 25-29, 31-33, 35-39, 41 and 42, including all entered amendments thereto, appears in the attached Appendix.

SUMMARY OF THE INVENTION

Embodiments of the present invention relate to a demodulator that can perform Quadrature Phase Shift Keying (QPSK) modulation and analog-to-digital conversion using only an analog-to-digital converter. (Specification, page 3, lines 13-15). In other words, embodiments of the present invention relate to separating components of a digital signal in an analog-to-digital converter. In embodiments, such a demodulator is power efficient and cost effective. (Specification, page 4, lines 1-3).

ISSUES

- Issue 1.** Whether the Examiner erred in the rejection of claim 1 under 35 U.S.C. § 102(e) because Chalmers (U.S. Patent No. 5,640,416) does not disclose “...an analog-to-digital converter device to convert an intermediate frequency signal into a digital signal and provides a quadrature component and an in-phase component of the digital signal...”
- Issue 2.** Whether the Examiner erred in the rejection of claim 21 under 35 U.S.C. § 102(e) because Efstathiou (U.S. Patent No. 6,504,867) does not disclose “...an analog-to-digital converter to convert an intermediate frequency CDMA signal to an intermediate digital signal and a channel separator to generate first and second digital signals based on the intermediate digital signal...”
- Issue 3.** Whether the Examiner erred in the rejection of claims 22-23, 25-29 and 31 under 35 U.S.C. § 102(e) because Chalmers (U.S. Patent No. 5,640,416) does not disclose “...separating components of [a] digital signal from the digital signal in [an] analog-to-digital converter...”

Issue 4. Whether the Examiner erred in the rejection of claims 32-33, 35-39 and 41 under 35 U.S.C. § 102(e) because Chalmers (U.S. Patent No. 5,640,416) does not disclose "...[a]n apparatus configured to...separate components of the digital signal from the digital signal in the analog-to-digital converter..."

Issue 5. Whether the Examiner erred in the rejection of claim 42 under 35 U.S.C. § 102(e) because Chalmers (U.S. Patent No. 5,640,416) does not disclose "...separating components of [a] digital signal from the digital signal in [an] analog-to-digital converter..."

GROUPING OF THE CLAIMS

Appealed claim 1 forms a single group and stands or falls independently. Appealed claim 21 forms a single group and stands or falls independently. Appealed claims 22-23, 25-29 and 31 form a single group and stand or fall together. Appealed claims 32-33, 35-39 and 41 form a single group and stand or fall together. Appealed claim 42 forms a single group and stands or falls independently.

THE ARGUMENT

Argument 1. The Examiner erred in the rejection of claim 1 under 35 U.S.C. § 102(e) because Chalmers does not disclose "...an analog-to-digital converter device to convert an intermediate frequency signal into a digital signal and provides a quadrature component and an in-phase component of the digital signal..." (emphasis added).

To establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must describe each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Also see M.P.E.P. § 2131.

Claim 1 recites "...an analog-to-digital converter device to convert an intermediate frequency signal into a digital signal and provides a quadrature component and an in-phase component of the digital signal..."

Chalmers relates to a digital downconverter/despreader for a direct sequence spread spectrum communications system. It is disclosed in column 7, lines 41-44 that A/D converter 406 samples IF signal 416. It is further disclosed that the output of A/D converter 406 is processed in custom digital IC 408. Specifically, it is disclosed in column 8, lines 22-23 that A/D converter 406 produces an aliased spectrum. An aliased spectrum is not a digital signal. In column 7, lines 56-60 it is disclosed that

the downconverter/despreader IC 408 processes the aliased spectrum to output digital data symbols. Accordingly, unlike the recitations of claims 1 and 5, A/D converter 406 does not convert an intermediate frequency into a digital signal. This is evident and apparent, as the output of A/D converter 406 is an aliased spectrum, as shown in Figure 6(b) of Chalmers. Figure 6(b) of Chalmers is not a digital signal.

A/D converter 406 also does not provide a quadrature component and an in-phase component of the digital signal. This is evident and apparent, as it is disclosed that downconverter/despreader IC 408 outputs in-phase and quadrature symbols from the output of A/D converter 406. In other words, downconverter/despreader IC 408 produces in-phase and quadrature symbols from an aliased signal and not from a digital signal.

In conclusion, the single prior art reference of Chalmers does not describe each and every element as set forth in claim 1. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Further, the identical invention of "...an analog-to-digital converter device to convert an intermediate frequency signal into a digital signal and provides a quadrature component and an in-phase component of the digital signal..." is not shown in as complete detail as is contained in claim 1. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). At least for these reasons, a *prima facie* case of anticipation has not been established under 35 U.S.C. § 102.

Argument 2. The Examiner erred in the rejection of claim 21 under 35 U.S.C. § 102(e) because Efstathiou does not disclose "...an analog-to-digital converter to convert an intermediate frequency CDMA signal to an intermediate digital signal and a channel separator to generate first and second digital signals based on the intermediate digital signal..." (emphasis added).

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Claim 21 recites "...an analog-to-digital converter to convert an intermediate frequency CDMA signal to an intermediate digital signal and a channel separator to generate first and second digital signals based on the intermediate digital signal..."

Efstathiou relates to digital matched filtering for signal estimation in a digital receiver. In Figure 1 and the accompanying description in column 3, lines 41-43, it is disclosed that analog-to-digital converter (ADC) 28 provides a wide band digitized signal on line 29. However, unlike the recitations of claim 21, ADC 28 is not disclosed as having a channel separator. This is evident and apparent, as it is disclosed in Figure 2 and the accompanying description in column 3, lines 55-64 that tuner 30 is configured to

provide an in-phase and quadrature signals. Accordingly, ADC 28 does not have a channel separator, as tuner 30 provides the function of providing in-phase and quadrature signals.

In conclusion, the single prior art reference of Efstathiou does not describe each and every element as set forth in claim 21. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Further, the identical invention of "...an analog-to-digital converter to convert an intermediate frequency CDMA signal to an intermediate digital signal and a channel separator to generate first and second digital signals based on the intermediate digital signal..." is not shown in as complete detail as is contained in claim 21. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). At least for these reasons, a *prima facie* case of anticipation has not been established under 35 U.S.C. § 102.

Argument 3. The Examiner erred in the rejection of claims 22-23, 25-29 and 31 under 35 U.S.C. § 102(e) because Chalmers does not disclose "...separating components of [a] digital signal from the digital signal in [an] analog-to-digital converter..."

To establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must describe each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Also see M.P.E.P. § 2131.

Claims 22-23, 25-29, and 31 recite "...separating components of [a] digital signal from the digital signal in [an] analog-to-digital converter..."

Chalmers relates to a digital downconverter/despreader for a direct sequence spread spectrum communications system. It is disclosed in column 7, lines 41-44 that A/D converter 406 samples IF signal 416. It is further disclosed that the output of A/D converter 406 is processed in custom digital IC 408. Specifically, it is disclosed in column 8, lines 22-23 that A/D converter 406 produces an aliased spectrum. An aliased spectrum is not a digital signal. In column 7, lines 56-60 it is disclosed that the downconverter/despreader IC 408 processes the aliased spectrum to output digital data symbols. Accordingly, unlike the recitations of claims 1 and 5, A/D converter 406 does not convert an intermediate frequency into a digital signal. This is evident and apparent,

as the output of A/D converter 406 is an aliased spectrum, as shown in Figure 6(b) of Chalmers. Figure 6(b) of Chalmers is not a digital signal.

A/D converter 406 also does not provide a quadrature component and an in-phase component of the digital signal. This is evident and apparent, as it is disclosed that downconverter/despreader IC 408 outputs in-phase and quadrature symbols from the output of A/D converter 406. In other words, downconverter/despreader IC 408 produces in-phase and quadrature symbols from an aliased signal and not from a digital signal.

In conclusion, the single prior art reference of Chalmers did not describe each and every element as set forth in claims 22-23, 25-29 and 31. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Further, the identical invention of "...separating components of [a] digital signal from the digital signal in [an] analog-to-digital converter..." is not shown in as complete detail as is contained in claims 22-23, 25-29, and 31. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). At least for these reasons, a *prima facie* case of anticipation has not been established under 35 U.S.C. § 102.

Argument 4. The Examiner erred in the rejection of claims 32-33, 35-39 and 41 under 35 U.S.C. § 102(e) because Chalmers does not disclose "...[an] apparatus configured to separate components of the digital signal from the digital signal in the analog-to-digital converter..."

To establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must describe each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Also see M.P.E.P. § 2131.

Claims 32-33, 35-39 and 41 recite "...[an] apparatus configured to separate components of the digital signal from the digital signal in the analog-to-digital converter..."

Chalmers relates to a digital downconverter/despreader for a direct sequence spread spectrum communications system. It is disclosed in column 7, lines 41-44 that A/D converter 406 samples IF signal 416. It is further disclosed that the output of A/D converter 406 is processed in custom digital IC 408. Specifically, it is disclosed in column 8, lines 22-23 that A/D converter 406 produces an aliased spectrum. An aliased spectrum is not a digital signal. In column 7, lines 56-60 it is disclosed that the downconverter/despreader IC 408 processes the aliased spectrum to output digital data symbols. Accordingly, unlike the recitations of claims 1 and 5, A/D converter 406 does

not convert an intermediate frequency into a digital signal. This is evident and apparent, as the output of A/D converter 406 is an aliased spectrum, as shown in Figure 6(b) of Chalmers. Figure 6(b) of Chalmers is not a digital signal.

A/D converter 406 also does not provide a quadrature component and an in-phase component of the digital signal. This is evident and apparent, as it is disclosed that downconverter/desreader IC 408 outputs in-phase and quadrature symbols from the output of A/D converter 406. In other words, downconverter/desreader IC 408 produces in-phase and quadrature symbols from an aliased signal and not from a digital signal.

In conclusion, the single prior art reference of Chalmers does not describe each and every element as set forth in claims 32-33, 35-39 and 41. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Further, the identical invention of "...[an] apparatus configured to separate components of the digital signal from the digital signal in the analog-to-digital converter..." is not shown in as complete detail as is contained in claims 32-33, 35-39 and 41. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). At least for these reasons, a *prima facie* case of anticipation has not been established under 35 U.S.C. § 102.

Argument 5. The Examiner erred in the rejection of claim 42 under 35 U.S.C. § 102(e) because Chalmers (U.S. Patent No. 5,640,416) does not disclose "...separating components of the digital signal from the digital signal in the analog-to-digital converter..."

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Claim 42 recites "...separating components of the digital signal from the digital signal in the analog-to-digital converter..."

Chalmers relates to a digital downconverter/despreader for a direct sequence spread spectrum communications system. It is disclosed in column 7, lines 41-44 that A/D converter 406 samples IF signal 416. It is further disclosed that the output of A/D converter 406 is processed in custom digital IC 408. Specifically, it is disclosed in column 8, lines 22-23 that A/D converter 406 produces an aliased spectrum. An aliased spectrum is not a digital signal. In column 7, lines 56-60 it is disclosed that the downconverter/despreader IC 408 processes the aliased spectrum to output digital data symbols. Accordingly, unlike the recitations of claims 1 and 5, A/D converter 406 does not convert an intermediate frequency into a digital signal. This is evident and apparent,

as the output of A/D converter 406 is an aliased spectrum, as shown in Figure 6(b) of Chalmers. Figure 6(b) of Chalmers is not a digital signal.

A/D converter 406 also does not provide a quadrature component and an in-phase component of the digital signal. This is evident and apparent, as it is disclosed that downconverter/despreader IC 408 outputs in-phase and quadrature symbols from the output of A/D converter 406. In other words, downconverter / despreader IC 408 produces in-phase and quadrature symbols from an aliased signal and not from a digital signal.

In conclusion, the single prior art reference of Chalmers does not describe each and every element as set forth in claim 42. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Further, the identical invention of "...separating components of the digital signal from the digital signal in the analog-to-digital converter..." is not shown in as complete detail as is contained in claim 42. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). At least for these reasons, a *prima facie* case of anticipation has not been established under 35 U.S.C. § 102.

CONCLUSION

The Appellant respectfully requests the Honorable Board of Appeals and Interferences of the U.S. Patent and Trademark Office to withdraw the rejections of claims 1, 21-23, 25-29, 31-33, 35-39, 41 and 42 because *prima facie* cases of anticipation under 35 U.S.C. § 102 and obviousness under 35 U.S.C. § 103 have not been established.

Respectfully submitted,
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APPENDIX

1. A demodulation apparatus for a communication system, comprising:
 - an analog-to-digital converter device to convert an intermediate frequency signal into a digital signal and provide a quadrature component and an in-phase component of the digital signal;
 - a plurality of filters to filter components of the digital signal outputted from the analog-to-digital converter device in a low pass band respectively; and
 - a CDMA modem to demodulate outputs of the plurality of filters.

21. A demodulator for a CDMA receiver, comprising:
 - an input circuit to amplify a filtered CDMA formatted input signal;
 - a first signal processor to generate an intermediate frequency CDMA signal based on the amplified input signal;
 - a second signal processor to output first and second digital signals on first and second channels, respectively, based on the intermediated frequency CDMA signal, said second signal processor having an analog-to-digital converter to convert the intermediate frequency CDMA signal to an intermediate digital signal and a channel separator to generate the first and second digital signals based on the intermediate digital signal; and
 - an output circuit to output a demodulated output signal based on the first and second digital signals, said output circuit having first and second Finite Impulse Response (FIR)

filters to receive and filter the first and second digital signals, respectively, wherein the first and second digital signals have different phases.

22. A method comprising:
converting an analog signal to a digital signal in an analog-to-digital converter; and
separating components of the digital signal from the digital signal in the analog-to-digital converter.

23. The method of claim 22, wherein the components of the digital signal are:
an in-phase component of the digital signal; and
a quadrature component of the digital signal.

25. The method of claim 22, wherein the analog signal embodies a CDMA communication signal.

26. The method of claim 23, wherein:
an in-phase component of the digital signal is associated with an in-phase component of the analog signal;
the quadrature component of the digital signal is associated with the quadrature component of the analog signal; and

the quadrature component of the analog signal is 90 degrees out of phase with the in-phase component of the analog signal.

27. The method of claim 22, wherein the converting the analog signal to the digital signal comprises:

sampling the analog signal to produce a sampled analog signal; and
quantizing the sampled analog signal to produce the digital signal.

28. The method of claim 27, wherein sampling the analog signal comprises sampling at a frequency that is four times the frequency of each component of the digital signal.

29. The method of claim 28, wherein the separating components of the digital signal from the digital signal comprises:

outputting on a first channel bits of the digital signal that are associated with the in-phase component of the digital signal; and

outputting on a second channel bits of the digital signal that are associated with the quadrature component of the digital signal.

31. The method of claim 30, wherein each bit of said bits of the digital signal that are associated with the in-phase component of the digital signal are preceding a bit of said of the digital signal that is associated with the quadrature component of the digital signal.

32. An apparatus configured to:
convert an analog signal to a digital signal in an analog-to-digital converter; and
separate components of the digital signal from the digital signal in the analog-to-digital converter.

33. The apparatus of claim 32, wherein the components of the digital signal are:
an in-phase component of the digital signal; and
a quadrature component of the digital signal.

35. The apparatus of claim 32, wherein the analog signal embodies a CDMA communication signal.

36. The apparatus of claim 32, wherein:
an in-phase component of the digital signal is associated with an in-phase component of the analog signal;
the quadrature component of the digital signal is associated with the quadrature component of the analog signal; and
the quadrature component of the analog signal is 90 degrees out of phase with the in-phase component of the analog signal.

37. The apparatus of claim 32, wherein to convert the analog signal to the digital signal comprises:

sampling the analog signal to produce a sampled analog signal; and
quantizing the sampled analog signal to produce the digital signal.

38. The apparatus of claim 32, wherein to sample the analog signal comprises sampling at a frequency that is four times the frequency of each component of the digital signal.

39. The apparatus of claim 38, wherein to separate components of the digital signal from the digital signal comprises:

outputting on a first channel bits of the digital signal that are associated with the in-phase component of the digital signal; and

outputting on a second channel bits of the digital signal that are associated with the quadrature component of the digital signal.

41. The apparatus of claim 40, wherein each bit of said bits of the digital signal that are associated with the in-phase component of the digital signal are preceding a bit of said of the digital signal that is associated with the quadrature component of the digital signal.

42. An apparatus comprising:

an analog-to-digital converter;

a means for converting an analog signal to a digital signal in the analog-to-digital converter; and

a means for separating components of the digital signal from the digital signal in the analog-to-digital converter.